CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) structure comprising:

an elevated device region having at least one semiconductor device located on a second semiconductor layer, wherein said elevated device region further comprises a source/drain junction which extends from the second semiconductor layer down to a first buried insulator layer that is located on an upper surface of a semiconductor substrate, said first buried insulator is separated from the second semiconductor layer by a first semiconductor layer and a second buried insulator layer;

a recessed device region having at least one semiconductor device located atop a first semiconductor layer which is located on an upper surface of the first buried insulator; and

an isolation region separating said elevated device region from said recessed device region.

2. The SOI MOSFET structure of Claim 1 wherein the elevated device region further comprises a merged source/drain region that is self-aligned to an edge of an isolation region and a spacer of a device located in the elevated device region.

3. The SOI MOSFET structure of Claim 1 wherein the elevated device region further comprises a merged source/drain region that is not self-aligned to an edge of an isolation region and a spacer of a device located in the elevated device region.

4. The SOI MOSFET of Claim 1 wherein the first semiconductor layer and the second semiconductor layer comprise the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge alloys, GaAs, InAs, InP, and other III/V or II/VI compound semiconductors.

5. The SOI MOSFET of Claim 4 wherein the first and the second semiconductor layers are strained, unstrained, or a combination of strained and unstrained.

6. The SOI MOSFET of Claim 4 wherein the first and second semiconductor layers are homogenous or heterogeneous layers.

7. The SOI MOSFET of Claim 4 wherein the first and second semiconductor layers have the same or different crystallographic orientation.

8. The SOI MOSFET of Claim 1 wherein the first semiconductor layer has a (100) crystallographic orientation and a device located thereon is an nFET, and the second semiconductor layer has a (110) crystallographic orientation and a device located thereon is a pFET.

9. The SOI MOSFET of Claim 1 wherein the first semiconductor layer has a (110) crystallographic orientation and a device located thereon is a pFET, and the second semiconductor layer has a (100) crystallographic orientation and a device located thereon is an nFET.

10. A method of forming a silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) structure comprising:

providing a structure comprising an elevated device region and a recessed device region that are separated from each other by an isolation region, said elevated device region comprising a first insulator layer located on a substrate, a first semiconductor layer

located on the first insulating layer, a second insulator layer located on the first semiconductor layer, and a second semiconductor layer located on the second insulator layer, and said recessed device region comprising said first buried insulator and said first semiconductor layer;

forming semiconductor devices in said elevated device region and said recessed device region, wherein the semiconductor device in the elevated device region is formed on the second semiconductor layer and the device in the recessed device region is formed on the first semiconductor layer;

forming merged source/drain regions in said elevated device region that lay on the first semiconductor layer; and

forming junctions in the elevated and recessed device regions, said junction in the recessed device region extends from an upper surface of the second semiconductor layer down to the first buried insulator layer.

11. The method of Claim 10 wherein said providing step includes a layer transfer process and wafer bonding.

12. The method of Claim 11 wherein said wafer bonding is performed in an inert ambient at a temperature from about 200° to about 400°C for a time period from about 2 to about 20 hours.

13. The method of Claim 11 wherein said providing step further includes forming a patterned etch mask on the second semiconductor layer in said elevated device region, selectively etching the second semiconductor layer and the second buried insulator layer in said recessed device area, and removing said patterned etch mask.

14. The method of Claim 10 wherein the first semiconductor layer has a (100) crystallographic orientation and the device formed thereon is an nFET, and the second semiconductor layer has a (110) crystallographic orientation and the device formed thereon is a pFET.

15. The method of Claim 10 wherein the first semiconductor layer has a (110) crystallographic orientation and the device formed thereon is a pFET, and the second semiconductor layer has a (100) crystallographic orientation and the device formed thereon is an nFET.

16. The method of Claim 10 wherein said merged source/drain region is self-aligned to an edge of an isolation region and a spacer of the device located in the elevated device region

17. The method of Claim 10 wherein said merged source/drain region is not self-aligned to an edge of an isolation region and a spacer of the device located in the elevated device region

18. The method of Claim 10 wherein said forming said merged source/drain regions comprises the steps of forming a patterned sacrificial mask atop of the recessed device region; removing exposed second semiconductor material, underlying second buried insulator layer stopping on a surface of the first semiconductor layer using a spacer of said device in said elevated device region and an isolation region as etch masks and filling the etched areas with a conductive material.

19. The method of Claim 10 wherein said forming said merged source/drain regions comprises the steps of forming an epi mask in the recessed device region; removing exposed second semiconductor material, underlying second buried insulator layer stopping on a surface of the first semiconductor layer using a spacer of said device in

said elevated device region and an isolation region as etch masks and filling the etched areas with a conductive material.

20. The method of Claim 10 wherein junctions are formed by ion implantation and annealing.